IN THE CLAIMS:

Please amend claims 1, 10, and 13 as indicated below.

Please add new claims 17-21.

1. (Currently Amended) A system, comprising:

a bus including a power line;

a bus bridge device including an internal logic unit; and

a power regulator to deliver power to the power line, the power regulator further to assert a fault signal to the bus bridge device if a power fault is detected on the bus, the bus bridge device to disconnect the internal logic unit from the bus in response to an assertion of the fault signal to prevent the internal logic unit from being corrupted with invalid data from the bus.

2. (Cancelled)

3. (Previously presented) The system of claim 1, the power regulator to cease to deliver power to the power line if a power fault is detected.

4. (Original) The system of claim 3, the bus bridge device to assert an interrupt signal in response to the assertion of the fault signal.

5. (Original) The system of claim 3, the bus bridge device to assert an error signal in response to the assertion of the fault signal.

6. (Original) The system of claim 3, the bus bridge device to assert a power enable signal to the power regulator upon system startup, the power regulator to deliver power to the power line in response to the assertion of the power enable signal.

7. (Original) The system of claim 6, the bus bridge device to deassert the power enable signal follow the assertion of the fault signal.

8. (Original) The system of claim 7, the power regulator module to deassert the fault signal in response to the deassertion of the power enable signal.

9. (Original) The system of claim 8, wherein the bus is a PCI bus.

10. (Currently Amended) A bus bridge device, comprising:

a bus interface unit ~~to coupled to~~ coupling the bus bridge device to a bus;

an internal logic unit coupled to the bus interface unit; and

a fault signal input coupled to receive a fault signal, the bus bridge device to disconnect the internal logic unit from the bus in response to an assertion of the fault signal to prevent the internal logic unit from being corrupted with invalid data from the bus.

11. (Original) The bus bridge device of claim 10, further comprising an interrupt signal output, the bus bridge device to assert the interrupt signal output in response to the assertion of the fault signal.

12. (Original) The bus bridge device of claim 10, further comprising an error signal output, the bus bridge device to assert the error signal in response to the assertion of the fault signal.

13. (Currently Amended) A method, comprising:

applying power to a bus;

detecting a power fault on the bus;

removing power from the bus; and

asserting a fault signal to a bus bridge device; and

disconnecting an internal logic unit within the bus bridge device from the bus in response to the assertion of the fault signal to prevent the internal logic unit from being corrupted with invalid data from the bus.

14. (Cancelled)

15. (Previously presented) The method of claim 13, further comprising asserting an interrupt signal in response to the assertion of the fault signal.

16. (Previously presented) The method of claim 13, further comprising asserting an error signal in response to the assertion of the fault signal.

17. (New) The system of claim 1, wherein the bus bridge device is to assert a power enable signal to the power regulator to enable the power regulator to deliver power to the bus when the power fault is not detected.

18. (New) The system of claim 17, wherein in response to the detected power fault, the bus bridge device is to de-assert the power enable signal to the power regulator to enable the power regulator stop delivering the power to the bus.

19. (New) The system of claim 18, wherein in response to the de-asserted power enable signal received from the bus bridge device, the power regulator is to de-assert the fault signal to the bus bridge device.

20. (New) The system of claim 19, wherein the power regulator is not to deliver the power to the bus again until the power enable signal is asserted by the bus bridge device.

21. (New) The system of claim 20, wherein the bus is a secondary PCI bus, wherein the bus bridge device is a PCI/PCI bridge bridging the secondary PCI bus to a primary PCI bus coupled to a processor via a system logic device, and wherein in response to the fault signal,

the PCI/PCI bridge is to assert an error signal to the system logic device regarding a fault condition associated with the fault signal,

the system logic device is to generate an interrupt to the processor, and

in response to the interrupt, the processor to invoke system software to perform a predetermined operation, including at least one of scheduling a system shutdown and alerting a system administrator regarding the fault condition.